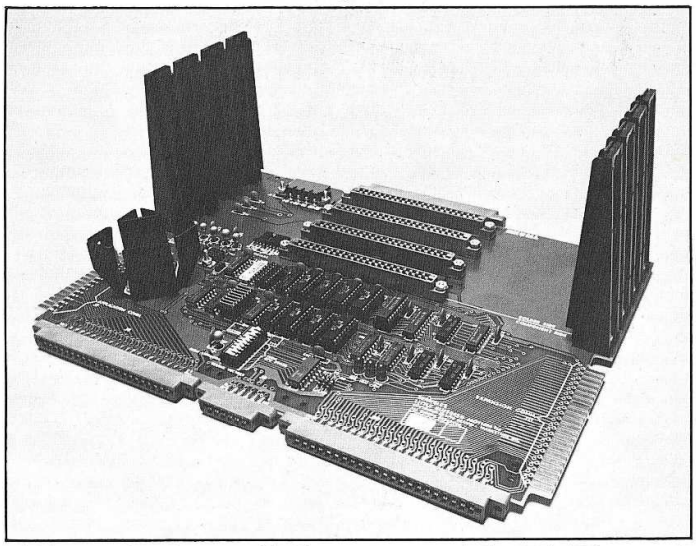
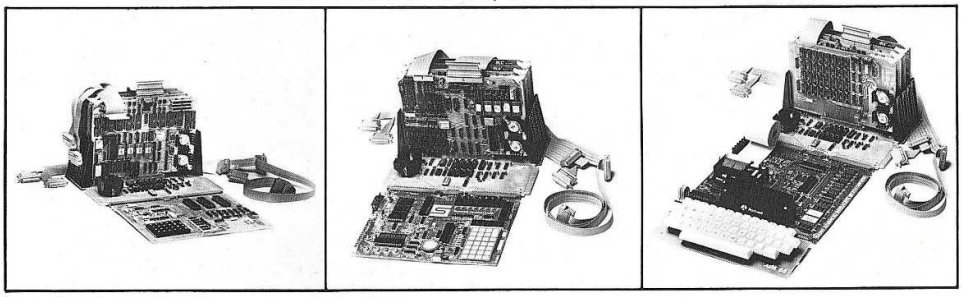
Introducing SEAWELL's



Little Buffered Mother

The ultimate Motherboard for any KIM-1, SYM-1, or AIM-65 system



Features:

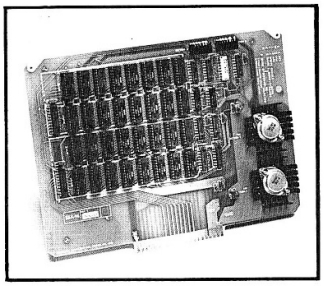
- 4K Static RAM on board
- +5V, +12V, and −12V regulators on board
- 4 + 1 buffered expansion slots
- Accepts KIM-4 compatible boards
- Full access to application & expansion connector
- LED indicators for IRQ, NMI, and power-on
- Also compatible with SEA-1, SEA-16, the PROMMER, SEA-PROTO, SEA-ISDC, and more
- Onboard hardware for optional use of A-17 (128K addressing limit)
- Mounts like KIM-4 or with CPU board standing up
- 10 slot Motherboard expansion available - SEAWELL's Maxi Mother

For further information contact:

SEAWELL Marketing Inc.
P.O. Box 17006
Seattle, WA 98107

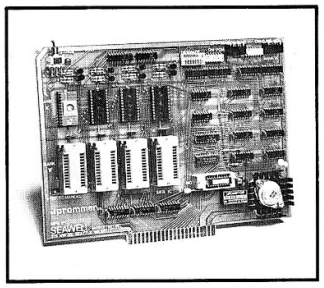
SEAWELL Marketing Inc.
315 N.W. 85th
Seattle, WA 98117
(206) 782-9480

Little Buffered Mother's Compatible Hardware



SEA-16/16

SEA-16/16 is a 16K x 8 Static RAM Board. Two individually addressable 8K blocks of RAM, with individual WRITE PROTECT and optional Bank Switching. SEA-16/8 is the same as above except 8K of RAM not installed.
SEA-16/BLANK is the same as above, except no RAM is installed, thirty two 2114's makes it go.



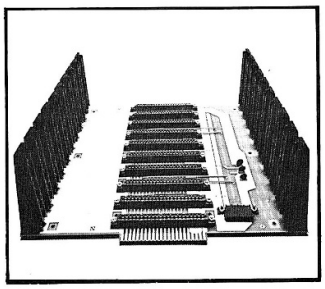
The Prommer

EpROM Programmer and EpROM/ROM Board. Memory mapped EpROM programming will program up to 16K per command, firmware in PROM included. Specify KIM, SYM or AIM.

All products are assembled. No kits.

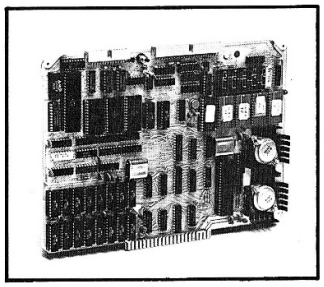
For further information contact:

SEAWELL Marketing Inc.
P.O. Box 17006
Seattle, WA 98107



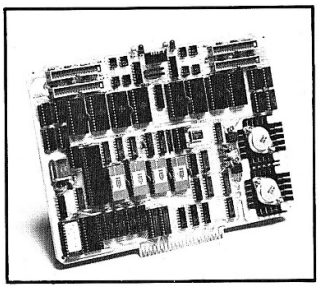
The Maxi-Mother

The Maxi-Mother® is a 10 slot Mother Board. Combined with the Little Buffered Mother®, it provides 14 slots or use it stand-alone with SEA-1.



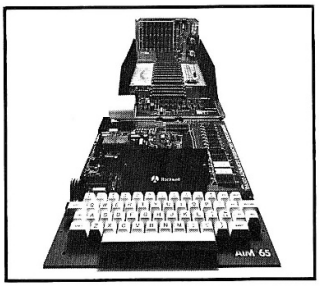
SEA-1 Seawell's CPU Board

MCS 6512 CPU, 3 Hardware RS-232 Ports, one current-loop, programmable Audio Tape interface, 9K + Static RAM, up to 18K of ROM/EpROM, Single Step Hardware, Bank Switching, Interrupt driven Monitor, and more.



SEA-ISDC Intelligent Serial Data Concentrator

MCS 6512 CPU, 4K of Dual Port RAM, 2K local RAM, 4K EpROM/ROM, 8 RS-232 Ports. The SEA-ISDC can operate as a stand-alone computer or as a buss compatible "Front End" I/0 Processor for a larger system. The 4K of RAM can be accessed by either CPU without delay.



Or go for the works!

AIM-65 with the Little Buffered Mother®, the Maxi-Mother® and SEA-16/16.

Available Soon!

Parallel 1/0 Board, Prototype Board and Floppy Disk Controller

SEAWELL Marketing Inc.
315 N.W. 85th
Seattle, WA 98117
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LITTLE BUFFERED MOTHER MANUAL

TABLE of CONTENTS

The concept of a mother board is familiar to most microcomputer users. In most cases the microprocessor is on one printed circuit board along with the system clock and the buffers or drivers that interface it to the buss. The processor board usually plugs into a mother board which serves only to interconnect it with the other boards in the system. In the case of the three popular 6502 based single board computers; the KIM-1 by Mos Technology, the SYM-1 by Synertek, and the AIM-65 by Rockwell, there are no onboard buffers. Many of the microprocessor outputs are loaded to the point that only half a TTL load can be added without exceeding the spec. This allows expansion provided that only the buffers are connected direcly to the expansion connector.

The expansion connector of the three computers are compatable, that is they have the same signals on corresponding pins. However, since the data buss is bidirectional its buffer must not be enabled when the microprocessor is reading onboard devices. Some address decoding, therefore, is required in order to control the data buss buffers. Since the three computers differ in their onboard decoding a versatile decoding system is required to adapt to all three. This versatile decoding is useful even if only one computer is to be used. It allows the user to select on or off board RESET and Interrupt and to adapt to the amount of onboard ROMs actually installed in the SYM or AIM.

All three computers have space for an additional 4K of RAM in the first 8K. The optional 4K of static RAM occupies this unused space as follows:

$400 to $1400 for the KIM
$1000 to $2000 for the SYM or AIM

Since most memory boards are 8K or larger and allow for addressing only in 8K blocks it is difficult to populate this memory space with available RAM boards.

The LITTLE BUFFERED MOTHER (LBM) provides for the most general possible expansion of the three computers. Filling in the first 8K of the memory map and buffering all the E-connector lines allows straightforward expansion in 8K blocks up to 65K. The provision for a bank select line allows for expansion beyond 65K and/or the ability to switch devices in and out of the memory map. The four board slots on the LBM are sufficient to expand with 16K RAM boards (SEA-16 or equivelent) or EPROM (the Prommer) to 65K. The connector on the back of the LBM allows further expansion of the mother board. The back connector can also be used as a board slot. Since the boards plug in component side up, it is usefull for testing or for odd sized special boards. The LBM performs several other useful functions. It has voltage regulators that provide +5 volts, +12 volts, and -12 volts from unregulated supplies. (It requires only the +5 volts itself). The LBM also has 3 LEDs indicating power, IRQ, and NMI. A KIM keybord/TTY switch is also provided.

SET-UP: The LBM is packed with the card guides detached. You will find eight card guides, screws, and nuts. Insert the screws from the bottom (solder side) of the mother board in the holes along the outside edge. The inner hole is for the locating pin on the card guide. Put the nuts on the screws 4 or 5 turns and, holding the screw heads against the bottom side of the board, slip the card guide into place and tighten the screw.

POWER: You will also find a power supply connector. Connect your power supply to the "Little Buffered Mother" tm. using the enclosed power connector. Individual contacts are supplied. The silkscreen markings by the power connector on the board can be used for reference. These are nominal unregulated voltages that connect directly to the expansion slots. See the SEABUS5 section for the detailed power requirements. +8 Volts is regulated to +5 on the LBM and connected to the CPU board. Only +8 is required by the LBM and the SYM. +16 is regulated at +12 and is required by the KIM to read tapes. -16 is regulated at -12 and connected to the SYM P-connector. -12 is optional for the SYM (see the SYM-1 Manual) The AIM requires +24 volts for its printer to operate. This must be supplied directly to the AIM through its own connector. Power supplies that are not required by your computer may be required by boards plugged into the SEABUS5 expansion slots. You may power up the LBM without connecting it to your computer. The RED "Power-on" LED will light.

CONNECTING THE CPU: Your CPU board mates directly to the LBM along the front edge. Both the "A" and "E" connectors (and for the SYM the "P" connector) mate simultaneously. With the power off, place both boards on a flat surface and bring them together, aligning the connectors. Hold down the LBM "E" connector and push the CPU "E" connector in part way, then do the same for the "A" connector, then the "E" again, etc., until both are firmly in place. If you have a SYM you will be mating 3 connectors at once.

HEADER: Find the 16 pin header in one of the two sockets nearest the voltage regulator heat sink. One socket is labeled "KIM", and the other "SYM/AIM". Put the header in the socket labeled with the name of your computer.

SWITCHES: There are 10 switches, all in one package. They are labeled on the board as follows:

The "KEYBOARD/TTY" switch is used only by the KIM to point the KIM monitor to the onboard keyboard display or the tty I/O port. It has no effect on the SYM or the AIM.

The next 8 switches counting toward the CPU board are labeled 8 through F. This is the most significant HEX digit of the 4K address blocks controlled by the switch. In the "open" position (labeled "from expansion") the data buss buffers are enabled for the corresponding

block of addresses and the 6502 is connected to the expansion connectors on the LBM. In the other position (labeled "from CPU board") the buffers are disabled and the 6502 addresses only its onboard devices. If the buffers are enabled for an address which is decoded by a device on the CPU board a conflict will result. Both the buffer and the device will attempt to put data on the buss at the same time, the LBM's buffers will override a MOS device and the 6502 will see only the data from the expansion buss whether or not there is a device at that address on the expansion buss. To avoid possible (but unlikely) damage to devices on the CPU board the LBMs switches should be carefully set to allow all CPU board devices control of the buss when they are addressed. All of the KIM's onboard hardware is accounted for by the header since it is all in the first 8K. The SYM and the AIM have no onboard decoding below $8000 except the 4K of RAM accounted for by the header.

Switch	KIM	SYM	AIM
8	OPEN	CLOSED (MONITOR)	OPEN
9	OPEN	OPEN *	OPEN
A	OPEN	CLOSED (I/O)	CLOSED (I/O)
B	OPEN	OPEN *	* BASIC
C	OPEN	OPEN *	* BASIC
D	OPEN	OPEN *	* ASSEMBLER
E	OPEN	OPEN *	CLOSED (MONITOR)
F	OPEN	OPEN *	CLOSED (MONITOR)

* If ROMs are installed in the sockets provided on the CPU boarde they may occupy some of this address space.

The last switch affects the last 8 bytes of memory $FFF8-FFFF in the same way as the previous 8 affect 4K blocks. The 6502 fetches its RESET and interrupt starting addresses from this block. Normally you will want to reset to the CPU board monitor so you will put the switch in the "FROM CPU BOARD" position. If, however, you want to reset to your own software on an expansion board you will put the switch in the other position. (Note that you should be sure that the CPU board is not also trying to supply the reset vectors. In the case of the KIM the LBM uses the "DECODE-ENABLE" line of the "A" connector to disable the KIM's decoding. The SYM has straps that allow the vectors to be fetched from any of the onboard sockets. The AIM fetches its vectors from its monitor ROM so the switch must point to the cpu board if a ROM is installed in the monitor socket.

APPLICATION CONNECTOR: If you normally have something connected to your application connector, it can simply be connected to the LBM connector labeled "A" perpendicular to your CPU "A" connector. Note that +12 volts appears on pin "A"-N if +16V is connected to the power connector. The LBM handles the KIM's DECODE-ENABLE "A"-K and TTY-ENABLE "A"-21 and V.

4K RAM: If you have the optional 4K RAM it is set to the appropriate address by the installation of the header in the correct socket for your computer. If you do not have the 4K of RAM you may use the address space through SEABUSS expansion conectors.

KIM-1: Put the header in the KIM socket. This puts the 4K of RAM from 400 to 1400 hex and connects the Decode Enable (A-k) line to the LBM decode logic. You should not ground pin A-k and you need not connect A-21 and A-v to enable the TTY port. You may add your own switch in parallel if you wish. All of the 4K block switches may be pointed to the expansion buss since the KIM has no on board devices above $2000. The vector switch may be pointed to the KIM (CPU) to reset to the KIM monitor or to ROMs decoded at $FFFA through FFFF on the expansion buss.

SYM-1: Put the header in the SYM/AIM socket. This puts the optional 4K of RAM into addresses $1000 to $2000. Since the SYM has no Decode Enable, the switches must be set to avoid a buss conflict with the SYM's onboard devices. For a standard SYM (i.e. as supplied by Synertek) set switch 8,A and Vector to "from CPU". The other switches may be set to "from expansion". If you want to Reset to your own software rather than the SYM monitor you must change a strap on the SYM and set the Vector switch to "from expansion". Similarly if you install additional ROM or EPROM in the sockets on the SYM and strap the SYM to address them you will need to set the corresponding switch to "from CPU".

AIM-65: Put the header in the SYM/AIM socket this puts the optional 4K of RAM at addresses $1000 to $2000. The switches must be set to avoid the I/O and software installed in the AIM. In general A,E,F, and Vector will point to the AIM ("from CPU"). If BASIC is installed B and C must point to the AIM and if the Assembler is installed D must point to the AIM. The AIM has no provision for off-board vectors so the Vector switch will always point to the AIM unless the monitor ROM is removed.

The LBM has four strap options related to the expansion buss. Two options concern the Bank Select line and the other two concern DMA and External Clock. Since the KIM-4 did not have a Bank Select line boards made for the KIM-4 buss ignore this line. All Seawell boards can be set to ignore Bank Select also. The DMA and External Clock straps should be left in the "normal" position unless you plug another CPU board (such as the SEA-1) into the buss.

The first Bank Select strap is located at the corner of the large heat sink nearest the center of the board. Since no corresponding signal is present on the "E" connector of the CPU, Bank Select may be controlled by the A-Connector PB0 or PB1 lines. If a strap is installed it connects PB0 or PB1 to the input of an inverter (center pin) that drives the Bank Select line. Since the 6522s or 6530s that drive the PB lines reset to inputs and the inverter input is pulled up the Bank Select line will be low unless it is specifically set by the CPU. If no strap is installed the Bank Select line will be low (bank 0). The second strap is located in the group of three next to the first card slot. It connects the output of the inverter to the buss. If it is removed the Bank Select line must be controlled by a board on the buss. Except for special applications this strap should be left in the normal position.

MASTER PIN LIST

COMPONENT SIDE (NUMBERS)		SOLDER SIDE (LETTERS)	
NAME	PIN	PIN	NAME
GND	1	A	GND
SYNC	2	B	AB0
READY	3	C	AB1
$\overline{\text{IRQ}}$	4	D	AB2
-15V	5	E	AB3
$\overline{\text{NMI}}$	6	F	AB4
$\overline{\text{RESET}}$	7	H	AB5
DB7	8	J	AB6
DB6	9	K	AB7
DB5	10	L	AB8
DB4	11	M	AB9
DB3	12	N	AB10
DB2	13	P	AB11
DB1	14	R	AB12
DB0	15	S	AB13
$\overline{\text{EX CLK}}$	16	T	AB14
+15V	17	U	AB15
$\overline{\text{DMA}}$	18	V	PHASE 2
+8V	19	W	R/W
+8V	20	X	PHASE 1
+8V	21	Y	BANK
GND	22	Z	GND

GND - GROUND
THIS IS THE POWER AND SIGNAL GROUND AND SHOULD BE CONNECTED TO THE FRAME GROUND AT NO MORE THAN ONE POINT.

SYNC (OUT) - OPCODE FETCH CYCLE
THIS LINE GOES HIGH DURING PHASE 1 THE OPCODE FETCH CYCLE. IT APPEARS ON THE BUSS WITH ONE LS TTL BUFFER DELAY FROM THE PROCESSOR.

READY (IN) - DATA READY
THE PROCESSOR WILL STOP ON ANY READ CYCLE IF READY IS PULLED LOW DURING PHASE 1 OR THE FIRST 100 NS (50 NS IF 2 MHZ) OF PHASE 2. THE "READY" LINE IS PULLED UP AND BUFFERED ON THE PROCESSOR BOARD.

$\overline{IRQ}$ (IN) - MASKABLE INTERRUPT REQUEST
ANY BOARD MAY PULL DOWN THE -IRQ LINE BUT THE INTERRUPTING BOARD MUST PROVIDE AN INTERRUPT STATUS BIT READABLE BY THE CONTROLLING PROCESSOR.

$\overline{NMI}$ (IN) - NON-MASKABLE INTERRUPT
THIS IS A NEGATIVE, EDGE TRIGGERED INPUT PULLED UP ON THE PROCESSOR BOARD. SINCE IT IS EDGE TRIGGERED NO INTERRUPT WILL OCCUR IF IT IS ALREADY LOW. AS WITH -IRQ, THE INTERRUPTING DEVICE MUST PROVIDE AN INTERRUPT STATUS BIT. -NMI MUST BE HELD LOW FOR AT LEAST 2 CYCLES FOLLOWING THE TRANSISITON FROM HIGH TO LOW.

$\overline{RESET}$ (IN) - SYSTEM RESET
THIS LINE MAY BE PULLED LOW BY ANY DEVICE. IT IS PULLED UP BY THE PROCESSOR BOARD.
THE PROCESSOR BOARD HOLDS DOWN RESET DURING POWER UP.

DB0-DB7- BI-DIRECTIONAL DATA BUS
DATA BUSS BUFFERS SHOULD HAVE LESS THAN 20 NS DELAY. EACH BOARD SHOULD PRESENT NO MORE THAN ONE TTL LOAD. (BOARDS WHICH PRESENT GREATER LOADS LIMIT EXPANDABILITY AND SHOULD BE COUNTED AS MORE THAN ONE BOARD FOR LOADING PURPOSES.) MOS INPUTS ARE NOT TO BE CONNECTED DIRECTLY TO THE BUSS.

EX CLK (IN) - PROCESSOR BOARD CLOCK ENABLE
ANY DEVICE THAT SOURCES THE CLOCKS ON THE BUSS MUST PULL THIS LINE LOW TO DISABLE THE PROCESSOR BOARD CLOCK DRIVERS. THIS LINE MAY CHANGE ONLY WHILE "READY" IS LOW.

DMA (IN) - DIRECT MEMORY ACCESS
THIS LINE IS PULLED LOW BY A DEVICE TO DISABLE THE PROCESSOR'S BUSS DRIVERS. -DMA MUST BE REQUESTED FROM AND GRANTED BY THE CONTROLLING PROCESSOR THROUGH A STATUS/CONTROL REGISTER TO ASSURE THAT ONLY ONE DEVICE DOES DMA AT A TIME.

POWER SUPPLIES -
THREE UNREGULATED SUPPLIES ARE REQUIRED. THEY ARE INTENDED TO SUPPLY ON-BOARD REGULATORS WHICH REQUIRE ABOUT 2 VOLTS OF MARGIN TO PROVIDE +12, +5 AND -12 VOLTS. THUS THE MINIMUM VOLTAGES FOR PROPER OPERATION ARE +14, +7, AND -14 VOLTS.
IN ORDER TO LIMIT POWER DISSIPATION IN THE ON-BOARD REGULATORS THE RMS VOLTAGES ARE LIMITED TO 16.5, 8.5, AND -16.5. THE REGULATORS WILL WITHSTAND 35V. PEAKS, BUT FAST-SLEWING VOLTAGES MUST BE AVOIDED.

AB0-AB15 ADDRESS BUS (OUT)
EACH BOARD SHOULD PRESENT NO MORE THAN 2 LS TTL LOADS. DMA ADDRESS BUSS DRIVERS MUST HAVE THE DRIVE CAPABILITY OF A 74367 (AT LEAST).

PHASE 1 - SYSTEM CLOCK
PHASE 2 THE DURATION OF THE TWO CLOCK PHASES (PHASE 1 AND PHASE 2) MUST BE EQUAL WITHIN 10%. THE CLOCKS MUST BE NON-OVERLAPPING WITH NOMINAL 5 NS NON-OVERLAP TIME TO PROVIDE FOR UNEQUAL GATE DELAYS. BOARDS WHICH SOURCE A SYSTEM CLOCK MUST HAVE DRIVE EQUAL TO A 74367.

R/W - READ (-WRITE)
THIS IS THE PROCESSOR R/W LINE. IT IS BUFFERED SIMILIARILY TO AN ADDRESS LINE.

BANK - BANK SELECT
THIS LINE IS CONTROLLED BY THE PROCESSOR BOARD OR THE CONTROLLING DEVICE (BY ACCESSING THE SWITCH DECODED ON THE PROCESSOR BOARD) AND ACTS AS AN EXTRA ADDRESS LINE. ITS DRIVE AND LOADING IS THE SAME AS AN ADDRESS LINE AND IT CHANGES STATE DURING PHASE 1. MEMORY AND DEVICES MAY BE ADDRESSED IN BANK=0, BANK=1, NEITHER, OR BOTH.

COMPATIBILITY: SEABUSS is compatible with boards designed for the KIM-4 BUSS on all but 4 pins.

The KIM-4 does not use (or even connect) three of them, but the boards use them to drive decode enable and to connect to regulated +5 Volts if they are used with the KIM-1 alone.

If these boards are used on the SEABUSS the traces to pins 16, 21, and "Y" MUST ! be cut. Be sure that pin 21 is not connected to pin Y. These are the only modifications necessary and the boards will still work in a KIM-4. Pin X is Phase 1 on the SEABUSS and Phase 2 (negated) on the KIM-4. This is only a subtle timing change and as far as we know does not affect the operation of any of the boards. NOTE that Seawell Prommers shipped before March 1 1979 will require these modifications.

Problem Solver Systems 8K Static RAM board also requires these these modifications prior to installation. Permanent damage is likely if these three modifications are not done.

WARRANTY

Your Little Buffered Mother is warrented for 3 months, all parts, labor and freight.

SERVICE

If you encounter any problems when initially installing or using your LBM please don't hesitate to call or drop us a note. Our telephones are normally open from 9 AM to 5 PM weekdays. If you are convinced you have a hardware problem and wish to return your LBM for service, pack the unit properly and send it to us with as accurate a description of the problem as possible. Please ship the LBM pre-paid since we do not accept freight collect shipments. If the unit is still under warranty it will be returned with your freight cost enclosed.

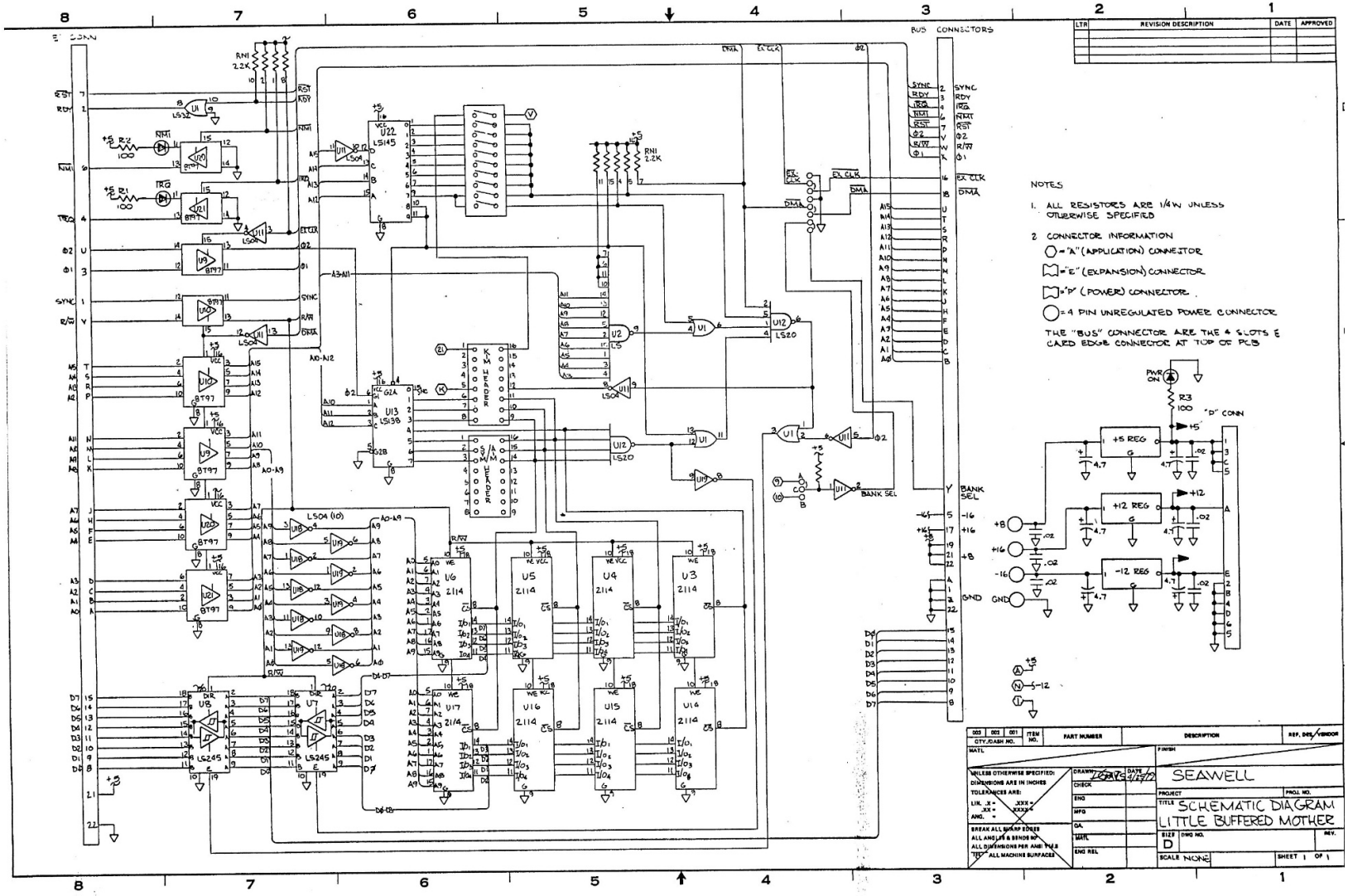
Our shipping address is:

SEAWELL MARKETING
315 N.W. 85th Street
SEATTLE, Wa 98117

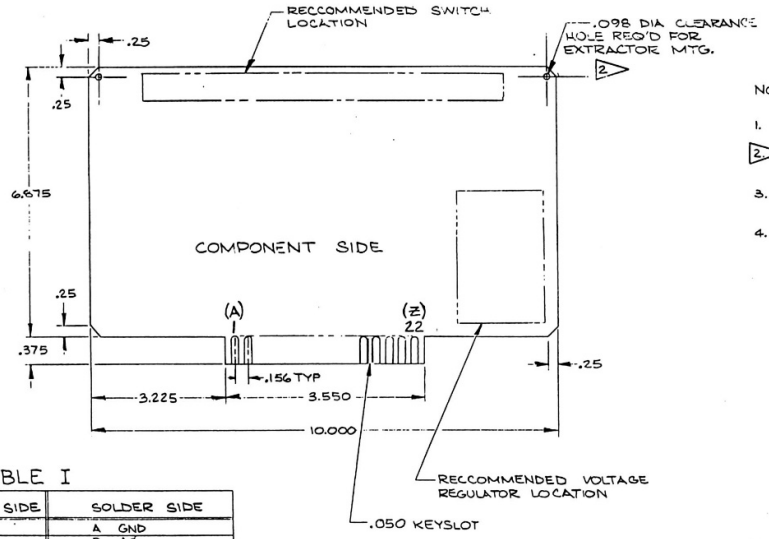
Our telephone number is:

(206) 782-9480

For service outside U.S. please contact our local representative.


BUS CONNECTORS
NOTES
1. ALL RESISTORS ARE 1/4W UNLESS OTHERWISE SPECIFIED
2 CONNECTOR INFORMATION
O = "A" (APPLICATION) CONNECTOR
= "E" (EXPANSION) CONNECTOR
= "P" (POWER) CONNECTOR
O = 4 PIN UNREGULATED POWER CONNECTOR
THE "BUS" CONNECTOR ARE THE 4 SLOTS E CARD EDGE CONNECTOR AT TOP OF PCB
+5 REG
+12 REG
-12 REG
"P" CONN
SEAWELL
SCHEMATIC DIAGRAM
LITTLE BUFFERED MOTHER
SIZE D
SCALE NONE
SHEET 1 OF 1

REVISIONS						
DWG REV	ZONE	DESCRIPTION	DWN	CK	APP	DATE



NOTES:

1. BOARD THICKNESS .062.
2. EXTRACTORS ARE TO BE BIVAR P/N CP-06 OR EQUIV.
3. RECCOMENDED MAX COMPONENT HEIGHT IS .500.
4. FOR CONNECTOR PIN DESIGNATIONS SEE TABLE I

TABLE I

COMPONENT SIDE		SOLDER SIDE	
1	GND	A	GND
2	SYNC	B	AØ
3	RDY	C	A1
4	IRQ	D	A2
5	-15V	E	A3
6	NMI	F	A4
7	RST	H	A5
8	D7	J	A6
9	D6	K	A7
10	D5	L	A8
11	D4	M	A9
12	D3	N	A10
13	D2	P	A11
14	D1	R	A12
15	DØ	S	A13
16	EX CLOCK	T	A14
17	+15V	U	A15
18	DMA	V	Ø2 (PHASE 2)
19	+8V	W	R/W
20	+8V	X	Ø1
21	+8V	Y	BANK SELECT
22	GND	Z	GND

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES NOT SPECIFIED ARE:
DECIMALS: ANGLES: ± ½°
XX ± .03
XXX ± .010
MATERIAL:
FINISH:
DO NOT SCALE DRAWING

APPROVALS		DATE
DRAWN	D GRAVES	
CHECKED		
ENGRG		
QC		
MFG ENG		
APP'D		

SEAWELL

TITLE: "SEABUS" COMPATIBLE PCB OUTLINE

CODE IDENT NO.	SIZE	DWG NO.
	C	cat. code

SCALE NONE SHEET 1 OF 1